Learning Outcomes based Curriculum Framework (LOCF)

For

Master of Technology
(Electronics and Communication Engineering)
Two Year Regular Full-Time
Postgraduate Programme

Faculty of Engineering and Technology
Chaudhary Devi Lal University
Sirsa-125055
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1. Faculty of Engineering & Technology

The Faculty covers the professional and academic programmes/courses run in the university teaching department of computer science and engineering, university school of graduate studies, affiliated general degree colleges, institute of computer applications and engineering colleges. BTech and MTech programmes in major disciplines and MCA, MSc Data Science, BSc Data Science, BCA programmes are managed by the Faculty.

2. Learning Outcome based Curriculum Framework

The CBCS evolved into learning outcome based curriculum framework and provides an opportunity for the students to choose courses from the prescribed courses comprising core, elective/minor or skill-based courses. The courses can be evaluated following the grading system, which is considered to be better than the conventional marks system. Grading system provides uniformity in the evaluation and computation of the Cumulative Grade Point Average (CGPA) based on student's performance in examinations which enables the student to move across institutions of higher learning. The uniformity in evaluation system also enables the potential employers in assessing the performance of the candidates.

2.1 Objectives of the programme

In today's global economic environment, engineers are required to play a vital role in bringing the prosperity to the nation. In this era of global village, the convergence of Electronics and Communication Technology is opening endless and exciting possibilities in almost every sphere of human activity. The M.Tech. programme in Electronics & Communication Engineering will cater the growing demands of technocrats in industry not only locally but also globally. There is huge potential for PG students in getting placements and to grow themselves in the diverse field of Electronics & Communication which includes Microelectronics, VLSI design, Wireless & Optical Communication, Advanced Digital Signal Processing, Embedded Systems, etc. After spending two years in the professional M.Tech. Electronics & Communication Engineering regular full-time programme, graduates are expected to:

- Exhibit support for peers and leadership by spearheading the projects teams; entrepreneurial skills by conceptualising new software projects; contributing to research and academia by way of undertaking research and academic assignments.
- Engage in lifelong learning, career enhancement and adapt to changing professional, societal, and environmental needs in a way conforming to his/her position in the profession/vocation;
- Develop communication skills necessary to function productively in the given settings to achieve a successful professional/vocational career with academic and professional ethics and social obligations.

2.2 Programme Outcomes (POs)

PO1	**gineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/Development of Solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct Investigations of Complex Problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data,

	and synthesis of the information to provide valid conclusions.
PO5	**Modern Tool Usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
PO6	**The Engineer and Society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and Sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and Team Work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
PO11	**oject Management and Finance:** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**fe-long Learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

2.3 Programme Specific Outcomes (PSOs)

The graduates of the Master of Technology Electronics & Communication Engineering programme will have/be:

PSO1	Ample knowledge of principles and practices of Electronics and Communication engineering and capability of putting these principles to use in solving relevant problems.
PSO2	Students should be able to develop advanced understanding of the concepts of Electronics & communication engineering and their applications in the specific areas of VLSI, Communication Engineering and signal processing
PSO3	Students should have an ability to apply technical knowledge of modern hardware & software tools for the design of electronic subsystems for solving various engineering problems.
PSO4	Working knowledge set for practicing their respective vocation/profession with ethics, integrity, leadership, and social responsibility.
PSO5	Equipped to achieve their career goals in the academia/industry or pursue higher studies and enhance their professional knowledge.

3. Programme Structure

Master of Technology ECE programme, a four-semester postgraduate programme is 78 credits weightage consisting of Core Courses (CC), Discipline Specific Elective Courses (DSC), Skill Enhancement Courses (SEC), and Open Elective Courses (OEC).

Table 1: Master of Technology ECE Credit Scheme

Sem	Core Courses (CC)		Discipline Specific Elective Courses (DSC)		Skill Enhancement Courses		Open Elective Courses (OEC)*		Grand Total Credits
	No. of Course	Total Credits	No. of Course	Total Credits	No. of Course	Total Credits	No. of Course	Total Credits	
I	4	12	02	08	-	-	-	-	20
II	4	12	02	08	-	-	1	4	24
III	3	10	-	-	1	4	1	4	18
IV	-	-	-	-	1	16	-	-	16
Total	11	34	04	16	02	20	02	08	78
%age	-	43.58	-	20.51	-	25.64	-	10.25	100

* A total of 08 credits are to be earned from other Engineering Departments or from MOOCs.

Table 2: Detailed break-up of Courses' Type (Semester wise)

Semester	Core Courses	Discipline Specific Elective Courses	Skill Enhancement Courses	Open Elective Courses	Total Courses
I	CC1 CC2 CC3 CC4	DSC1 DSC2	-	-	6
II	CC5 CC6 CC7 CC8	DSC3 DSC4	-	OEC1	7
III	CC9 CC10 CC11	-	SEC1	OEC2	5
IV	-	-	SEC2	-	1

Table 3: Courses' codes, titles, and credits

Course Code	Course Title	Contact Hours/Credit		
	Semester I	L	P	Total
MTech/ECE/1/CC1	Embedded System Design	4/4	-	4/4
MTech/ECE/1/CC2	Hardware Description Language	4/4	-	4/4
MTech/ECE/1/DSC1(i)	IC Fabrication Technology	4/4	-	4/4
MTech/ECE/1/DSC1(ii)	Advanced Computer Architecture			
MTech/ECE/1/DSC1(iii)	Memory system design			
MTech/ECE/1/DSC2(i)	Mobile communication	4/4	-	4/4
MTech/ECE/1/DSC2(ii)	Satellite communication			
MTech/ECE/1/DSC2(iii)	RF Microelectronics			
MTech/ECE/1/CC3	Hardware Description Language Lab	-	4/2	4/2
MTech/ECE/1/CC4	Embedded System Design Lab	-	4/2	4/2

Semester II				
MTech/ECE/2/CC5	Adaptive Signal Processing	4/4	-	4/4
MTech/ECE/2/CC6	Digital VLSI Design	4/4	-	4/4
MTech/ECE/2/DSC3(i)	Advanced Optical Communication	4/4	-	4/4
MTech/ECE/2/DSC3(ii)	Wireless Networks			
MTech/ECE/2/DSC3(iii)	Advancement in communication system			
MTech/ECE/2/DSC4(i)	Embedded system for wireless and mobile communication	4/4	-	4/4
MTech/ECE/2/DSC4(ii)	Signal processing			
MTech/ECE/2/DSC4(iii)	MEMS & IC Integration			
MTech/ECE/2/CC7	Digital VLSI Design lab	-	4/2	4/2
MTech/ECE/2/CC8	Adaptive Signal Processing Lab	-	4/2	4/2
MTech/ECE/2/OEC1	Students shall complete a 4-credit open elective course offered by other Engineering Departments/MOOCs	4/4	-	4/4
Semester III				
MTech/ECE/3/CC9	Advance digital communication	4/4	-	4/4
MTech/ECE/3/CC10	Research Methodology	4/4	-	4/4
MTech/ECE/3/CC11	Communication system design lab	-	4/2	4/2
MTech/ECE/3/SEC1	Dissertation Part-1	-	8/4	8/4
MTech/ECE/3/OEC2	Students shall complete a 4-credit open elective course offered by other Engineering Departments/MOOCs	4/4	-	4/4
Semester IV				
MTech/ECE/4/SEC2	Dissertation Part-2	-	32/16	32/16
	TOTAL	**48/48**	**60/30**	**108/78**

Table 4: M.Tech. Electronics & Communication Engineering Courses' List

Course Code	Course Title	Credits
Core Courses		
MTech/ECE/1/CC1	Embedded System Design	4
MTech/ECE/1/CC2	Hardware Description Language	4
MTech/ECE/1/CC3	Hardware Description Language Lab	2
MTech/ECE/1/CC4	Embedded System Design Lab	2
MTech/ECE/2/CC5	Adaptive Signal Processing	4
MTech/ECE/2/CC6	Digital VLSI Design	4
MTech/ECE/2/CC7	Digital VLSI Design lab	2
MTech/ECE/2/CC8	Adaptive Signal Processing Lab	2
MTech/ECE/3/CC9	Advance digital communication	4
MTech/ECE/3/CC10	Research Methodology	4
MTech/ECE/3/CC11	Communication system design lab	2
Discipline Specific Elective Courses		
MTech/ECE/1/DSC1(i)	IC Fabrication Technology	4
MTech/ECE/1/DSC1(ii)	Advanced Computer Architecture	

MTech/ECE/1/DSC1(iii)	Memory system design	
MTech/ECE/1/DSC2(i)	Mobile communication	4
MTech/ECE/1/DSC2(ii)	Satellite communication	
MTech/ECE/1/DSC2(iii)	RF Microelectronics	
MTech/ECE/2/DSC3(i)	Advanced Optical Communication	4
MTech/ECE/2/DSC3(ii)	Wireless Networks	
MTech/ECE/2/DSC3(iii)	Advancement in communication system	
MTech/ECE/2/DSC4(i)	Embedded system for wireless and mobile communication	4
MTech/ECE/2/DSC4(ii)	Signal processing	
MTech/ECE/2/DSC4(iii)	MEMS & IC Integration	
Skill Enhancement Courses		
MTech/ECE/3/SEC1	Dissertation Part-1 (Internal evaluation)	4
MTech/ECE/4/SEC2	Dissertation Part-2	16
Open Elective Courses		
MTech/ECE/2/OEC1	Students shall complete a 4-credit open elective course offered by other Engineering Departments/MOOCs	4
MTech/ECE/3/OEC2	Students shall complete a 4-credit open elective course offered by other Engineering Departments/MOOCs	4
Open Electives Courses offered to the students of other departments		
ECE/OEC1	Advancements in Communication Systems	4
ECE/OEC2	Wireless Communication	4

First Semester

MTech/ECE/1/CC1 **Embedded System Design**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Compulsory Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Microprocessor, Basic of C language, Analog & Digital circuits

Course Objectives:

1. To impart in-depth knowledge related to the architecture, interfacing and programming concepts of 8051 micro-controller.
2. To provide thorough coverage to advanced and state-of-the-art micro-controllers like ARM, AVR, PIC and JTAG.
3. To familiarize students with the concepts and techniques of Embedded System Project Management.

Course Outcomes:

CO-1 Understating of detailed architecture of conventional as well as the latest microcontroller.

CO-2 Develop assembly language programs for problem Solvay related to embedded systems.

CO-3 Ability to design and implement an embedded system using model circuits design.

CO-PO Mapping Matrix for Course MTech/ECE/1/CC1

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	1	3	1	1	-	-	-	-	2	3
CO2	3	1	1	3	3	1	-	-	-	-	3	3
CO3	3	3	1	3	1	1	-	-	-	-	3	3

UNIT-1

Introduction to Embedded systems design: Introduction to Embedded system, Embedded System Project Management, ESD and Co-design issues in System development Process, Design cycle in the development phase for an embedded system. Use of target system or its emulator and In-circuit emulator, Use of Software tools for development of an ES.

UNIT-2

8051 Microcontroller: Microprocessor V/s Micro-controller, 8051 Microcontroller: General architecture; Memory organization; I/O pins, ports & circuits; Counters and Timers; Serial data input/output; Interrupts.

UNIT-3

8051 Instructions: Addressing Modes, Instruction set: Data Move Operations, Logical Operations, Arithmetic Operations, Jump and Call Subroutine, Advanced Instructions. 8051

Interfacing and Applications: Interfacing External Memory, Keyboard and Display Devices: LED, 7-segment LED display, LCD.

UNIT-4

Advanced Microcontrollers: Only brief general architecture of AVR, PIC and ARM microcontrollers; JTAG: Concept and Boundary Scan Architecture.

Text Books:

1. Embedded Systems by Raj Kamal, TMH.
2. The 8051 Microcontroller by K.J. Ayala, Penram International.
3. J B Peatman, Design with PIC Microcontrollers, Prentice Hall.

References Books:

1. An Embedded Software Primer by David E. Simon, Pearson Education.
2. Designing Embedded Hardware by John Catsoulis, O'reilly
3. Embedded System Design by Frank Vahid, Tony Givargis," John Wiley & Sons, Inc
4. Building Embedded Linux Systems by KarimYaghmour, O'reilly
5. Programming Embedded Systems by Michael Barr, O'reilly
6. Real-time systems & software by Alan C. Shaw, John Wiley & sons, Inc.
7. Computers as Components by Wayne Wolf, Harcourt India Pvt. Ltd.
8. Embedded System Design by Peter Marwedel, Kluwer Academic Pub.
9. Programming and Customizing the AVR Microcontroller by DhananjayGadre, MGH
10. Fundamental of Embedded software by Daniel W. Lewis, PHI
11. Bluetooth Technology by CSR Prabhu& A.P. Reddi, PHI
12. John B Peat man "Design with Microcontroller ", Pearson education Asia, 1998
13. Burns, Alan and Wellings, Andy, "Real-Time Systems and Programming Languages", Second Edition. Harlow: Addison-Wesley-Longman, 1997
14. Raymond J.A. Bhur and Donald L.Bialey, " An Introduction to real time systems: Design to networking with C/C++ ", Prentice Hall Inc. New Jersey, 1999
15. Grehan Moore, and Cyliax, " Real time Programming: A guide to 32 Bit Embedded Development. Reading "Addison-Wesley-Longman, 1998
16. Heath, Steve, "Embedded Systems Design ", Newnes 1997

MTech/ECE/1/CC2 **Hardware Description Languages**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Compulsory Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Digital Electronics

Course Objective: This course is for first year post graduation students. This course is designed to make students learn VHDL that is one of the popular hardware descriptive languages. The course begins with the introduction of Hardware design and Design Methodologies. Basic and advanced concepts required to write a VHDL code are covered in detail. At the end a brief Introduction of Another popular hardware descriptive language Verilog is included.

Course Outcomes:

CO-1 Gain knowledge of hardware design methodologies using VHDL & Verilog.

CO-2 Ability to white VHDL code in various modelling styles i.e. structural, behavioral and sequential.

CO-3 Ability to develop circuits and projects for professional development.

CO-PO Mapping Matrix for Course MTech/ECE/1/CC2												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	1	3	1	1	-	-	-	-	2	3
CO2	3	1	1	3	3	1	-	-	-	-	3	3
CO3	3	3	1	3	1	1	-	-	-	-	3	3

UNIT-1

Introduction to Hardware Design: Digital System Design Process, Hardware Description Languages, Hardware Simulation, Hardware Synthesis, Levels of Abstraction.

VHDL Background: VHDL History, Existing Languages, VHDL Requirements, the VHDL Language.

UNIT-2

Design Methodology Based On VHDL: Elements of VHDL, Top down Design, Top down Design with VHDL, Subprograms, Controller Description, VHDL Operators, Conventions and Syntax.

Basic Concepts In VHDL: Characterizing Hardware Languages, Objects and Classes, Signal Assignments, Concurrent and Sequential Assignments.

UNIT-3

Design Organization and Parameterization: Definition and Usage of Subprograms, Packaging

Parts and Utilities, Design Parameterization, Design Configuration, Design Libraries.
Utilities For High-Level Descriptions: Type Declarations and Usage, VHDL Operators, Subprogram Parameter Types and Overloading, Other Types and Type Related Issues, Predefined Attributes, User Defined Attributes.

UNIT-4

Dataflow Descriptions In VHDL: Multiplexing and Data Selection, State Machine Description, Three State Bussing.
Behavioral Description of Hardware: Process Statement, Assertion Statement, Sequential Wait Statements, Formatted ASCII I/O Operations, MSI Based Design.

Verilog: Overview of Digital design with Verilog HDL, Hierarchical modeling concepts, basic concepts, modules & ports.

Text Books:

1. J. Bhasker, A VHDL Primer, Third Edition, PH/Pearson, 1999.
2. J. Bhasker, A VHDL Synthesis Primer, Second Edition, Star Galaxy, 1998.
3. J. Bhasker, A Verilog HDL Primer, Second Edition, Star Galaxy, 1999.
4. J. Bhasker, A Verilog Synthesis: A Practical Primer, Star Galaxy, 1998.
5. M. J. S. Smith, Application Specific Integrated Circuits, AW/Pearson, 1997.

Reference Books:

1. Z. Navabi, VHDL: Analysis and Modeling of Digital Systems, Second Edition, MH, 1998.
2. J. Armstrong and F. G. Gray, VHDL Design Representation and Synthesis, Second Edition, PH/Pearson, 2000.
3. P. J. Ashenden, The Designer's Guide to VHDL, Second Edition, Morgan Kaufmann, 2001.
4. D. Naylor and S. Jones, VHDL: A Logic Synthesis Approach, Chapman & Hall, 1997.
5. J. Pick, VHDL: Techniques, Experiments and Caveats, MH, 1996.
6. C. H. Roth, Digital System Design with VHDL, PWS/Brookscole, 1998.
7. M. G. Arnold, Verilog Digital Computer Design: Algorithms to Hardware, PH, 1999.
8. Z. Navabi, Verilog Digital System Design, MH, 1999.
9. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, PH/Pearson, 1996.
10. D. E. Thomas and P. R. Moorby, the Verilog Hardware Description Language, Fourth Edition, Kluwer, 1998.
11. K. Coffman, Real World FPGA Design with Verilog, PH, 2000.
12. D. R. Smith and P. D. Franzon, Verilog Styles for Synthesis of Digital Systems, AW/Pearson, 2001.
13. S. M. Trimberger, FPGA Technology, Kluwer, 1992.
14. J. V. Oldfield and R. C. Dorf, FPGAs: Reconfigurable Logic for RapidPrototyping and Implementation of Digital Systems, Wiley, 1995.
15. R. C. Seals and G. F. Whapshott, Programmable Logic: PLDs and FPGAs, MH, 1998.
16. A.K. Sharma, Programmable Logic Handbook: PLDs, CPLDs and FPGAs, MH, 1998.

MTech/ECE/1/CC3 **Hardware Description Languages Lab**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Practical	02	04	Lab Work	50	-	3 Hours	TEE/ Practical File
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Digital Electronics

Course Objective:

This course is for first year post graduation students. This course is designed to give students in-hand practice of writing and simulating a VHDL code. VHDL is one of the popular hardware descriptive language. Various combinational and sequential circuits like simple logic gates, Half Adder, Full Adder, Multiplexer, Demultiplexer, Encoder, decoder, Flip-Flops, Shift Register, Counters are included.

Course Outcomes:

CO-1 Understanding of system and concepts required to write a UHDL code.
CO-2 Ability to simulate UHDL code and develop circuits models.
CO-3 Ability to identify and debug system and logical problems.
CO-4 Ability to address research challenges through circuits analysis and modelling.

CO-PO Mapping Matrix for Course MTech/ECE/1/CC3												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	2	-	-	-	-	1	2
CO2	2	1	1	3	1	1	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3
CO4	3	3	1	3	1	1	-	-	-	-	3	3

List of Experiments

1. Design all gates using VHDL.
2. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
    a) Half adder
    b) Full adder
3. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
    a) Multiplexer
    b) Demultiplexer
4. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
    a) Decoder

    b) Encoder
5. Write a VHDL program for Single –Bit ALU and check the wave forms and the hardware generated
6. Write a VHDL program for a comparator and check the wave forms and the hardware generated
7. Write a VHDL program for a code converter and check the wave forms and the hardware generated
8. Write a VHDL program for a 9-bit parity generator and check the wave forms and the hardware generated
9. Write a VHDL program for a FLIP-FLOP and check the wave forms and the hardware generated.
10. Write a VHDL program for a counter and check the wave forms and the hardware generated.
    a) 3-bit binary counter
    b) 3-bit Up-Down counter
    c) Decade counter
11. Write VHDL programs for the following circuits, check the wave forms and the hardware generated
    a) register
    b) shift register
12. Implement any three (given above) on FPGA/CPLD kit

Note: This list is an indicative list of experiments, which can be expanded depending on the course requirement.

MTech/ECE/1/CC4 **Embedded System Design Lab**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Practical	02	04	Lab Work	50	-	3 Hours	TEE/ Practical File
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: C languages & basic of digital and analog circuits

Course Objectives:

1. To provide hand-on experience to the students on the industry standard KEIL make embedded Development boards related to 8051, PIC, ARM7, ARM9 processors.
2. To provide students an opportunity to understand the architecture of latest micro-controllers through programming using KEIL software and development boards.
3. To familiarize students with the interfacing of various application boards with development boards.

Course Outcomes:

CO-1 Practical understanding of architect use, interfacing issues and programming skills of latest microcontroller.

CO-2 Hands on experience on industry standard KEIL make development boards related to 8051, PIC, ARM and ARM9 processors.

CO-3 Develop assembly long programs for problem solving as well as interfacing of eternal devices with microcontroller.

CO-4 Ability to design and develop an imbedded system for variety of applications.

CO-PO Mapping Matrix for Course MTech/ECE/1/CC4

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	-	-	-	-	-	1	3
CO2	2	1	1	3	1	-	-	-	-	-	2	3
CO3	3	1	1	3	3	-	-	-	-	-	3	3
CO4	3	3	1	3	1	-	-	-	-	-	3	3

List of Experiments

1. (a) To familiarize with main features and concepts of programming in KEIL µvision software.
   (b) To familiarize with the architecture of 8051 micro-controller.
2. To write and run 8051 assembly language program to perform addition (8 & 16 bit) operation.
3. To write and run 8051 assembly language program to perform signed and unsigned subtraction operation. Also demonstrate the use of overflow flag.
4. To write and run 8051 assembly language program to perform MUL & DIV operations.
5. To write and run 8051 assembly language program to demonstrate all kind of MOV instructions, Stack related instructions and Data exchange.

6. To write and run 8051 assembly language program to demonstrate all kind of Logical operations along with certain exceptions.
7. To familiarize with architecture of 8051 development board and interfacing with PC to glow on-board LEDs.
8. To write and run C and 8051 assembly language program to glow on-board LEDs in 8051 development board with varying delay and patterns.
9. To interface 7-segment LED display with 8051 development board.
10. To interface LCD display with 8051 development board.
11. To practice basic assembly language programs of ARM using KEIL µvision software.

Note: This list is an indicative list of experiments, which can be expanded depending on the course requirement.

MTech/ECE/1/DSC1(i) **IC Fabrication Technology**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Microelectronics

Course Objectives: This is the very first course for the post-graduate students. This course first gives the knowledge of the necessary environment conditions for the integration technology. All the fabrication processes are then discussed step-by step which includes wafer cleaning, wet etching, ion implantation, oxidation, lithography, chemical Vapour deposition, metal film deposition, etching and then safe packaging.

Course Outcomes:

CO-1 Understanding of different techniques and measures for IC fabrication.
CO-2 Ability to apply fabrication principles in industry as a fabrication engineer.
CO-3 Ability to contribute for further research in IC fabrication.

CO-PO Mapping Matrix for Course MTech/ECE/1/DSC1(i)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	1	2	1	1	-	-	-	-	1	1
CO2	3	1	1	3	1	2	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3

UNIT-1

Environment for VLSI Technology: Clean room and safety requirements. Wafer cleaning processes and wet chemical etching techniques.

Impurity incorporation: Solid State diffusion modelling and technology; Ion Implantation modelling, technology and damage annealing; characterization of Impurity profiles.

UNIT-2

Oxidation: Kinetics of Silicon dioxide growth both for thick, thin and ultrathin films. Oxidation technologies in VLSI and ULSI; Characterizations of oxide films; High k and low k dielectrics for ULSI.

Lithography: Photolithography, E-beam lithography and newer lithography techniques for VLSI/ULSI; Mask generation.

UNIT-3

Chemical Vapour Deposition techniques: CVD techniques for deposition of polysilicon, silicon dioxide, silicon nitride and metal films; Epitaxial growth of silicon; modelling and

technology.

Metal film deposition: Evaporation and sputtering techniques. Failure mechanisms in metal interconnects; Multi-level metallization schemes.

UNIT-4

Plasma and Rapid Thermal Processing: PECVD, Plasma etching and RIE techniques; RTP techniques for annealing, growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technology.

Texts/References Books:

1. S.K. Gandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1994(2nd Edition).
2. S.M. Sze (Ed), VLSI Technology, 2nd Edition, McGraw Hill, 1988.
3. Plummer, Deal, Griffin "Silicon VLSI Technology: Fundamentals, Practice & Modeling" PH, 2001.
4. P. VanZant, "Microchip Fabrication", 5th Edition, MH, 2000.

MTech/ECE/1/DSC1(ii) **Advance Computer Architecture**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Basics of digital electronics and computer organization

Course Objectives:

Understand the architecture of a modem computer with its various processing units and the performance measurement of the computer system. The course also provides knowledge about memory management system of computer.

Course Outcomes:

At the end of the semester, students will be able to:

CO-1 Define& describe the terminology and fundamental principlesrelated to advanced computer architectures.

CO-2 Understand & explain parallel compute rmodels,advanced/multiprocessor architecture, memory designs/architecture.

CO-3 Demonstrate computer models and architecture, networkproperties , memory organizations and architecture .

CO-4 Analyze & evaluate the significance of pipelining, interconnect ions, memory hierarchy organizations and protocols.

CO-5 **Design** memory hierarchy, static and dynamic interconnectionnetworks.

CO-PO Mapping Matrix for Course MTech/ECE/1/DSC1(ii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	1	-	-	-	-	1	3
CO2	2	1	1	3	1	1	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3
CO4	3	3	1	3	1	1	-	-	-	-	3	3
CO5	3	1	1	1	3	1	-	-	-	-	3	3

UNIT-1

Parallel computer models: The state of computing, Classification of parallel computers, Multiprocessors and multi computers, Multivector and SIMD computers.

Program and network properties: Conditions of parallelism, Data and resource Dependences, Hardware and software parallelism, Program partitioning and scheduling, Grain Size and latency, Program flow mechanisms, Control flow versus data flow, Data flow Architecture, Demand driven mechanisms, Comparisons of flow mechanisms

UNIT-2

System Interconnect Architectures: Network properties and routing, Static interconnection Networks, Dynamic interconnection Networks, Multiprocessor system Interconnects, Hierarchical bus systems, Crossbar switch and multiport memory, Multistage and combining network.

Advanced processors: Advanced processor technology, Instruction- set Architectures, CISC Scalar Processors, RISC Scalar Processors, Superscalar Processors, VLIW Architectures, Vector and Symbolic processors Pipelining: Linear pipeline processor, nonlinear pipeline processor, Instruction pipeline Design, Mechanisms for instruction pipelining, Dynamic instruction scheduling, Branch Handling techniques, b ranch prediction, Arithmetic Pipeline Design, Computer arithmetic principles, Static Arithmetic pipeline, Multifunctional arithmetic pipelines.

UNIT-3

Memory Hierarchy Design: Cache basics & cache performance, reducing miss rate and miss penalty, multi level cache hierarchies, main memory organizations, design of memory hierarchies.

Multiprocessor architectures: Symmetric shared memory architectures, distributed shared memory architectures, models of memory consistency, .cache coherence protocols (MSI, MESI, MOESI), scalable cache coherence, overview of directory based approaches, design challenge of directory protocols,· memory based directory protocols, cache based directory protocols, protocol design tradeoffs, synchronization.

UNIT-4

Scalable point -point interfaces: Alpha364 and HT protocols, high performance signaling layer.

Enterprise Memory subsystem Architecture: Enterprise RAS Feature set: Machine check. hot add/remove, domain partitioning, memory mirroring/migration, patrol scrubbing, fault tolerant system.

Text Books:

1. Kai Hwang, "Advanced computer architecture";TMH.
2. D.A. Patterson, "Computer organization and design,"Morgan Kaufmann, 2nd Ed.

References:

1. J.P. Hayes, "Computer Architecture and organization"; MGH.
2. Harvey G. Cragon, "Memory System and Pipelined processors"; Narosa Publication.
3. V.Rajaranam & C.S.R. Murthy, "Parallel Computer" PHI.
4. R.K.Ghose, Rajan Moona & Phalguni Gupta, "Foundation of Parallel Processing Narosa Publications.
5. Kai Hwang and Zu, "Scalable Parallel Computers Architecture"; MGH.
6. Stalling W, "Computer Organisation & Architecture"; PHI.
7. D.Sima, T. Fountain, P. Kasuk, "Advanced Computer Architecture- Design space Approach,"Addison Wesley, 1997.
8. M.J Flynn, "Computer Architecture, Pipelined and Parallel Processor Design"; Narosa Publishing.
9. D.A. Patterson, J.L. Hennessy," Computer Architecture: A quantitative approach"; Morgan Kauffmann Feb,2002.

MTech/ECE/1/DSC1(iii) **Memory System Design**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Digital Circuit Design

Course Objectives:

This course is for Second year post graduation students. This course is designed for memory system organization, memory technologies, and characterization techniques for memory for low power.

Course Outcomes:

CO-1 Ability to demonstrate characterization and mathematical modeling
CO-2 Ability to understand various memory system organization.
CO-3 Ability to understand advance application based ultra-low power memory circuits.

CO-PO Mapping Matrix for Course MTech/ECE/1/DSC1(iii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	2	1	1	2	1	-	-	-	-	1	3
CO2	2	1	1	3	1	1	-	-	-	-	2	3
CO3	3	3	1	3	3	1	-	-	-	-	3	3

UNIT-1

Introduction to Memory Chip Design: Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Basic Operation of The 1-T Cell, Basic Operation of a SRAM Cell, Trends in Non-Volatile Memory Design and Technology, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology,

Basics of RAM Design and Technology: Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.

UNIT-2

DRAM Circuits: High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, W rite and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.

UNIT-3

On-Chip Voltage Generators: Substrate-Bias Voltage (VBB) Generator, Voltage Up-Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.

High-Performance Subsystem Memories: Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.

UNIT-4

Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.

Ultra-Low-Voltage Memory Circuits: Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low-Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.

Text Books:

1. K. Itoh, "VLSI Memory Chip Design', Springer, 2001.

MTech/ECE/1/DSC2(i) **Mobile Communication**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment / Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Communication System

Course Objectives:

1. To develop basic understanding and impart in-depth knowledge of various concepts used in wireless mobile communication.
2. To introduce the concepts, parameters and models of mobile radio propagation.
3. To help students understand the architecture and elements of wireless standards and systems like GSM, GPRS, CDMA, etc.
4. To provide coverage to the advanced, latest and upcoming wireless technologies like OFDM, Multicarrier Modulation, 4-G, Turbo codes and Multi-user detection, etc.

Course Outcomes:

CO-1 Develop thorough understanding of the advanced concepts used in wireless communication i.e. Mobile tail propagation, wireless system and analysis Diversity, etc.

CO-2 In-depth knowledge of the latest and future technologies prevalent in mobile communication industry i.e. Multicarrier, u-u, MUD, MIMO, etc.

CO-3 Develop interest/acumen to pursue further research in the area of broadband wireless comm.

CO-PO Mapping Matrix for Course MTech/ECE/1/DSC2(i)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	2	-	-	-	-	2	3
CO2	2	1	1	3	1	2	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3

UNIT-1

Introduction to Wireless Communication Systems: Various Generations of wireless mobile communication, The Cellular Concept, Frequency reuse, channel assignment strategies, hand-off strategies, interference and system capacity, improving capacity of cellular system through cell splitting, sectoring, etc.

UNIT-2

Mobile Radio Propagation: Introduction to radio wave propagation, three basic propagation mechanisms, Outdoor & indoor propagation models, small scale multipath propagation, parameters of mobile multipath channel, small scale & large scale fading, their types. **Principles of GSM:** GSM frequency bands, GSM architecture, GSM Interfaces, GSM logical channels and frame structure, GSM bursts, GPRS.

UNIT-3

CDMA System Concepts: Basics of CDMA. Spread spectrum concept. time hopping, Direct Sequence and Frequency Hopped Spread Spectrum, Chirp spread spectrum systems, Hybrid systems, Spreading sequences and their correlation functions, Code generation, Properties and generation of PN sequences, RAKE receiver, Diversity techniques an Rake receiver, Soft handoffs.

UNIT-4

Implementation Issues: OFDM, Multi-Carrier Modulation and Demodulation, Channel Coding and Decoding (Convolutional codes, Turbo codes), Multi-user Detection: Decorrelating detector, MMSE detector. Successive Interference Canceller, Parallel Interference Canceller.

Text Books:

1. Mobile Cellular Telecommunications; 2nd ed.; William, C Y Lee McGraw Hill
2. Wireless and Digital Communications; Dr. Kamilo Feher (PHI)
3. Principles of Mobile Communication, G.L. Stuber Kluwer Academic, 1996
4. Wireless Communication; Principles and Practice; T.S. Rappaport

MTech/ECE/1/DSC2(ii) **Satellite Communication**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Communication System

Course Objectives:

Satellite Communication Systems play a vital role in the global telecommunication system. It provides an essential and economical fixed and mobile communication services over broad coverage areas of land, sea and air. The course goal for Satellite Communications is to provide the student with the basic understanding and an in-depth knowledge of various concepts used in a satellite communication system. In this course, you will learn the about the science behind the orbiting satellites, link design and calculation, various multiplexing schemes and earth station parameters used for satellite communication. In the end various applications of satellite communication will be discussed.

Course Outcomes:

CO-1 Ability to demonstrate an understanding of the basic principles of satellite orbits, placement and control, satellite link design and the communication system components.

CO-2 Ability to specify systems design and analyze the performance of satellite communications systems.

CO-3 Ability to implement the satellite communication techniques for industry, social problems etc.

CO-PO Mapping Matrix for Course MTech/ECE/1/DSC2(ii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	1	-	-	1	-	1	3
CO2	1	1	1	3	1	1	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3

UNIT-1

Orbital Parameters: Orbital parameters, Orbital perturbations, Geo stationary orbits, Low Earth and Medium orbits. Frequency selection, Frequency co-ordination and regulatory services, Sun transit outages, Limits of visibility, Attitude and orientation control, Spin stabilization techniques, Gimbal platform

UNIT-2

Link Calculations: Space craft configuration, Payload and supporting subsystems, Satellite uplink - down link power budget, C/No, G/T, Noise temperature, System noise, Propagation factors, Rain and ice effects, Polarization calculations

Earth Station Parameters: Earth station location, propagation effects of ground, High power transmitters-Klystron Crossed field devices, Cassegrania feeds, Measurements on G/T and Eb/No

UNIT-3

Access Techniques: Modulation and Multiplexing: Voice, Data, Video, Analog and Digital transmission systems, multiple access techniques: FDMA, TDMA, T1-T2 carrier systems, SPADE, SS-TDMA, CDMA, Assignment Methods, Spread spectrum communication, Compression-Encryption and Decryption techniques

UNIT-4

Satellite Applications: INTELSAT Series, INSAT, VSAT, Remote sensing, Mobile satellite service: GSM. GPS, INMARSAT, Satellite Navigation System, Direct to Home service (DTH), Special services, E- mail, Video conferencing and Internet connectivity

Text Books:

1. Bruce R. Elbert," The Satellite Communication Applications Hand Book, Artech House Boston, 1997.
2. Wilbur L. Pritchard, Hendri G. Suyderhood, Robert A. Nelson, "Satellite Communication Systems Engineering" ,II Edition, Prentice Hall, New Jersey.1993
3. Dennis Rody," Satellite Communication", Regents/Prentice Hall, Eaglewood Cliff, New Jersey, 1983
4. Tri T. Ha, "Digital satellite communication", 2nd Edition, McGraw Hill, New york.1990
5. K. Feher, Digital communication satellite / Earth Station Engineering, prentice Hall Inc., New Jersey, 1983

MTech/ECE/1/DSC2(iii) **RF Micro-electronics**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Analog Electronics

Course Objectives:

This Course is for the Second year post-graduate students. The objective of this course is to provide students with understanding of modern RF electronics devices employed in RF Transceiver Design. This course is aimed to provide the knowledge of various issues encountered in high-frequency circuits, such as impedance matching, realization of passive components and bandwidth enhancement. Design components of radio-frequency systems, including low noise amplifiers, oscillators, mixers and power amplifiers will be discussed in detail. The effect of individual components performance on overall radio-frequency transmitter and receiver design and performance are also covered in this course plan.

Course Outcomes:

CO-1 Ability to understand the architectures, operation and performance specifications, tradeoff of a RF receiver and its building blocks.

CO-2 Ability to design and analyze various building blocks of receiver like filters, LNA, Mixer, Power Amplifiers, and VCO as per the specifications.

CO-3 Ability to understand the sources of nonlinearity, noise, process technology and its impact on the performance parameters of individual blocks of receiver and on receiver performance.

CO-PO Mapping Matrix for Course MTech/ECE/1/DSC2(iii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	2	1	1	1	-	-	-	-	2	2
CO2	2	1	1	2	1	1	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3

UNIT-1

Introduction to RF and Wireless Technology: Complexity, design and applications. Choice of Technology.

Basic concepts in RF Design: Nonlinearly and Time Variance, intersymbol Interference, random processes and Noise. Definitions of sensitivity and dynamic range, conversion Gains and Distortion.

UNIT-2

Analog and Digital Modulation for RF circuits: Comparison of various techniques for power efficiency. Coherent and Non coherent defection. Mobile RF Communication systems and basics

of Multiple Access techniques. Receiver and Transmitter Architectures and Testing heterodyne, Homodyne, Image-reject, Direct-IF and sub-sampled receivers. Direct Conversion and two steps transmitters. BJT and MOSFET behavior at RF frequencies Modeling of the transistors and SPICE models. Noise performance and limitation of devices. Integrated Parasitic elements at high frequencies and their monolithic implementation.

UNIT-3

Basic blocks in RF systems and their VLSI implementation: Low Noise Amplifiers design in various technologies, Design of Mixers at GHz frequency range. Various Mixers, their working and implementations, Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design. Quadrature and single-sideband generators.

UNIT-4

Radio Frequency Synthesizes: PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifiers design. Linearisation techniques, Design issues in integrated RF filters. Some discussion on available CAD tools for RF VLSI designs.

Texts/Reference Books:

1. B. Razavi, R F Microelectronics, Prentice-Hall PTR,1998
2. T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 1998.
3. R.Jacob Baker, H.W.i, and D.E. Boyce, CMOS Circuit Design Layout and Simulation, Prentice-Hall of India,1998.
4. Y.P. Tsividis Mixed Analog and Digital VLSI Devices and Technology, McGraw Hill,1996.

Second Semester

MTech/ECE/2/CC5 **Adaptive Signal Processing**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Compulsory Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Signals and Systems, Digital Signal Processing

Course Objectives:

To introduce the concepts and techniques associated with the understanding of digital signal processing. To familiarize with techniques suitable for analyzing and synthesizing both continuous-time and discrete time systems. To provide with an appreciation of applications for the techniques and mathematics used in this course.

Course Outcomes:

CO-1 Ability to understand the significance of signal processing (DSP) in the fields of computing, telecommunications and

CO-2 Ability to gain an appreciation of the technology and the software tools currently available

CO-3 Ability to study in detail some of the most important design techniques for DSP systems.

CO-PO Mapping Matrix for Course MTech/ECE/2/CC5

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	1	-	-	-	-	1	3
CO2	2	1	1	3	1	1	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3

UNIT-1

Basic Of Digital Signal Processing: Signals and Information, Signal Processing Methods, Applications of Digital Signal Processing, Derivation of the z-Transform Properties of z-Transform, Fourier series and Fourier transform. Random variable, Stochastic processes.

UNIT-2

Design of Digital Filters: Introduction, Linear Time-Invariant Digital Filters, Recursive and Non-Recursive Filters, Filtering Operation, Sum of Vector Products, A Comparison of Convolution and Correlation, Filter Structures, Direct, Cascade and Parallel Forms, Linear Phase FIR Filters Design of Digital FIR Filter-banks, Sub-band Filters, Design of Infinite Impulse Response IIR filters, Issues in the Design and Implementation of a Digital Filter.

UNIT-3

Estimation Theory: Bayesian Estimation Theory, Basic Definitions, Bayesian Estimation, Expectation Maximization Method, Generalized Parameter Estimation, Cramer–Rao lower Bound on the variance of estimator, maximum likelihood estimation, Design of Gaussian Mixture Models, Bayesian Classification, Modeling the Space of a Random Process, Detection **Adaptive Filtering:** State-Space Kalman Filters, Recursive Least Square (RLS) Adaptive Filters the Steepest-Descent Method LMS Filter, Different Algorithms and their Variants used in adaptive filtering and their performance criterion, Multirate Signal Processing.

UNIT-4

Applications: Applications of adaptive Digital Signal Processing to Speech, Music and Telecommunications, Parameter estimation, System identification, Noise and Echo cancellation, Acoustic source localization techniques, Channel Equalization**.**

Text Books:

1. Siomon S Haykins, "Adaptive Filter Theory," PHI, 3rd Edition
2. Proakis,"Digital Signal Processing," PHI 2nd edition
3. Harry L. Van Trees, "Detection, Estimation, and Modulation Theory, Part 1&3," Wiley 2002
4. Saeed V. Vaseghi, "Advanced Digital Signal Processing and Noise Reduction," Third Edition,2006
5. Eberhard Hänsler, "Gerhard Schmidt Acoustic Echo and Noise Control: A Practical Approach," Wiley, 2005.

MTech/ECE/2/CC6 **Digital VLSI Design**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Compulsory Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Digital Electronics

Course Objectives: This course is intended to be used for the first year post- graduate students. This course aims at covering first the basic building block of the VLSI circuits, that is, MOSFET and then the design equations for MOS, transistor sizing, various logic circuits design using MOS transistor. Memory designs and layouts are also covered under this course.

Course Outcomes:

CO-1 Understanding of building blocks of VLSI circuits and design equations.
CO-2 Gain knowledge of design principles and layouts of various logic circuits.
CO-3 Ability to identify and analyze problems in digital VLSI circuits.
CO-4 Apply subject knowledge of digital circuit design through software tools for advanced research.

CO-PO Mapping Matrix for Course MTech/ECE/2/CC6

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	1	1	1	1	-	-	-	-	1	3
CO2	2	2	1	3	1	1	-	-	1	-	2	3
CO3	2	1	1	3	3	1	-	-	-	-	3	3
CO4	2	3	1	3	1	1	-	-	-	-	3	3

UNIT-1

Introduction to MOSFETs: MOS Transistor Theory - Introduction MOS Device, Fabrication and Modeling, Body Effect, Noise Margin; Latch-up.

UNIT-2

MOS Inverter : MOS Transistors, MOS Transistor Switches, CMOS Logic, Circuit and System Representations, Design Equations, Static Load MOS Inverters, Transistor Sizing, Static and Switching Characteristics; MOS Capacitor; Resistivity of **V**arious Layers.

Symbolic and Physical Layout Systems: MOS Layers Stick/Layout Diagrams; Layout Design Rules, Issues of Scaling, Scaling factor for device parameters.

UNIT-3

Combinational MOS Logic Circuits: Pass Transistors/Transmission Gates; Designing with transmission gates, Primitive Logic Gates; Complex Logic Circuits.

Sequential MOS Logic Circuits: SR Latch, clocked Latch and flip flop circuits, CMOS D latch and edge triggered flip flop.

UNIT-4

Dynamic Logic Circuits: Basic principle, non-ideal effects, domino CMOS Logic, high performance dynamic CMOS Circuits, Clocking Issues, Two phase clocking.

CMOS Subsystem Design: Semiconductor memories, memory chip organization, RAM Cells, dynamic memory cell.

Text books:

1. S. M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Third Edition, MH, 2002.

Reference books:

1. W. Wolf, Modern VLSI Design: System on Chip, Third Edition, PH/Pearson, 2002.
2. N. Weste, K. Eshraghian and M. J. S. Smith, Principles of CMOS VLSI Design: A Systems Perspective, Second Edition (Expanded), AW/Pearson, 2001.
3. J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Digital Integrated Circuits: A Design Perspective, Second Edition, PH/Pearson, 2003.
4. D. A. Pucknell and K. Eshraghian, Basic VLSI Design: Systems and Circuits, Third Edition, PHI, 1994.
5. J. P. Uyemura, CMOS Logic Circuit Design, Kluwer, 1999.
6. J. P. Uyemura, Introduction to VLSI Circuits and System, Wiley, 2002.
7. R. J. Baker, H. W. Li and D. E. Boyce, CMOS Circuit Design, Layout and Simulation, PH, 1997.

MTech/ECE/2/CC7 **Digital VLSI Design Lab**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Practical	02	04	Lab Work	50	-	3 Hours	TEE/ Practical File
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Digital Electronics, knowledge of various ICs

Course Objectives:

This course aims at covering first the basic building block of the VLSI circuits, that is, start with MOSFET characteristics and then go through various logic circuits design using MOS transistor (like CMOS inverter, NAND NOR, MUX, DFF, Register) to complete Memory designs and layouts are also covered under this course.

Course Outcomes:

CO-1 Ability to characterize and model the circuit behaviors.

CO-2 Ability to apply theoretical concepts of digital VLSI design in practice through simulation tools.

CO-3 Develop logic circuits using MOS transistors, memory design and layout.

CO-4 Ability to work with industry standard simulation on tools and become a successful design engineer.

CO-PO Mapping Matrix for Course MTech/ECE/2/CC7												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	1	-	-	-	-	-	3
CO2	1	1	3	2	1	1	-	-	-	-	2	1
CO3	3	1	1	2	3	1	-	-	-	-	3	3
CO4	3	3	1	3	1	1	-	-	-	-	3	3

List of Experiments

1. Device Characterization
   Description: For the NMOS transistor simulate, observe and calculate the following
1. Using DC Sweep analysis, plot the ID Vs VDS and ID Vs VGS characteristics for
   a. Keeping the L = 0.18um, for W = 0.18um, 0.36um, 0.5um, 1um
   b. Keeping the W/L constant, say 1, for L = 0.18um, 0.36um, 0.5um, 1um
   2. From the ID Vs VDS plots generated in 1 above, for each of the case calculate the value of, channel length modulation parameter
   3. Measure the value of VT0
   4. Calculate Kn for NMOS Transistor
   5. Measure _ (Gamma), the body effect Parameter
2. Design and simulate the CMOS Inverting amplifier

Description: For the CMOS Inverter simulate, observe and calculate the following

1. Using DC Sweep analysis, plot the Vin VsVout CMOS inverter characteristics For:
   a) With the consideration of a Minimum Size inverter in a given Technology.
   b) Keeping the L = 0.18um, for W = 0.18um, 0.36um
   c) Plot the Drain Current in 1.a and 1.b
   d) Determine the noise margins.
2. Using transient analysis with an input pulse of 200MHz taking size as 1.a and 1.bsimulate the input/output switching characteristics.
   a) Measure the propagation delays.
3. Design and simulate the CMOS NAND/NOR/XOR gates
4. Design and simulate the CMOS 4x1 Mux and 1-bit Full Adder
5. Design and simulate the CMOS SR Latch and D-FF
6. Design and simulate the CMOS Non-Overlapping two phase Clock
7. Design and simulate the CMOS 6T SRAM Cell
8. Design and simulate the CMOS 4x4 SRAM

Note: This list is an indicative list of experiments, which can be expanded depending on the course requirement.

MTech/ECE/2/CC8 **Adaptive Signal Processing Lab**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Practical	02	04	Lab Work	50	-	3 Hours	TEE/ Practical File
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Basic of MATLAB, Concept of DSP

Course Objectives:

This course is designed to demonstrate the use of MATLAB software for simulation, synthesis and designing of different processing systems. Apart from this working with the DSP processor hardware is familiarized.

Course Outcomes:

CO-1 Ability to understand various algorithms related to windowing techniques.
CO-2 Ability to understand tools for the design of practical applicable filters.
CO-3 Ability to understand application based signal processing systems.

CO-PO Mapping Matrix for Course MTech/ECE/2/CC8												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	1	1	2	2	-	-	-	-	1	1
CO2	3	1	1	3	1	3	1	-	-	-	2	2
CO3	1	1	1	3	3	1	-	-	-	-	3	3

List of Experiments

1. Write Matlab statement for algebraic equations.
2. Designing filters from Windowing techniques.
3. Write Matlab program to find the Power spectral Density.
4. Matlab Program for plotting different graphs.
5. Filter design with the help of Matlab filter design tool.
6. Simulation of the given model using Simulink tool.
7. Matlab program for cross correlation and auto correlation.
8. Working with DSP Processor &Hardware.

Note: This list is an indicative list of experiments, which can be expanded depending on the course requirement.

MTech/ECE/2/DSC3(i) **Advanced Optical Communication Systems**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Physics of optical communication components and applications to communication systems

Course Objectives:

This course deals with the understanding of the optical components and the design and operation of optical fiber communication systems. The principles of wavelength division multiplexed (WDM) systems, SONET, SDH and passive optical networks. The characteristics and limitations of system components (laser diodes, external modulators, optical fiber, optical amplifiers, optical receivers) and the factors affecting the performance of the optical communication systems.

Course Outcomes:

CO-1 Thorough understating of the optical components and design of optical comm. System.

CO-2 Analysis of performances of optical filer comm. System and calculation of various performance parameters of optical link.

CO-3 Ability to apply concepts of optical comm. In further research for last mile affordable connectivity.

CO-PO Mapping Matrix for Course MTech/ECE/2/DSC3(i)

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	1	1	1	1	-	-	1	1	1	3
CO2	2	1	1	3	1	2	-	-	-	-	2	2
CO3	3	1	1	3	3	1	-	-	-	-	3	3

UNIT-1

Review: Evolution of Basic Fiber Optic Communication System, Benefits and disadvantages of Fiber Optics, Transmission Windows, Transmission Through Optical Fiber, The Numerical Aperture (NA), The Optical Fiber, Types of Fiber, Different Losses & Issues in Fiber Optics, Attenuation in Optical Fibers, Fiber Optic Loss Calculations, Dispersion, connectors & splices, bending loses, Absorption, scattering, very low loss materials, plastic & polymer-clad-silica fibers. Wave propagation in step index & graded index fiber, fiber dispersion, single mode fibers, multimode fibers, dispersion shifted fiber, dispersion flattened fiber, polarization, cut-off condition and V-parameter.

UNIT-2

Fiber Optic System Design Considerations and Components: Indoor Cables, Outdoor Cables, Cabling Example, Power Budget, Bandwidth and Rise Time Budgets, Electrical and Optical

Bandwidth, Connectors, Fiber Optic Couplers.
Dispersion and Nonlinearities Dispersion in single mode and multimode fibers, dispersion shifted and dispersion flattened fibers, attenuation and dispersion limits in fibers, Kerr nonlinearity, self phase modulation, Cross Phase Modulation, FWM.

UNIT-3

Optical Sources: optical source properties, operating wavelength of optical sources, semiconductor light-emitting diodes and laser diodes, semiconductor material and device operating principles, light-emitting diodes, surface-emitting LEDS, edge-emitting LEDS, super luminescent diodes, laser diodes, comparison of LED and ILD. Fiber optic transmitters, basic optical transmitters, direct versus external modulation, fiber optic transmitter applications.
Optical Detectors: Basic Information on light detectors, Role of an optical detector, Detector characteristics: Responsivity, Noise Equivalent Power, Detectivity, Quantum efficiency, The PN junction photo diode - PIN photodetectors - Avalanche photo diode construction characteristics and properties, APD Specifications, Applications of APD, Optical Receivers .

UNIT-4

Advanced Multiplexing Strategies: Optical TDM, subscriber multiplexing (SCM), WDM and Hybrid multiplexing methods.
Optical Networking: Data communication networks, network topologies, MAC protocols, Network Architecture- SONET/TDH, optical transport network, optical access network, optical premise network.

Text Books:
1. G.P. Aggrawal, Fiber-Optic Communication Systems, Wiley-Interscience.
2. G. Keiser, Optical Fiber Communication, Tata –McGraw Hill.
3. John Gowar, Optical communication systems, PHI.

MTech/ECE/2/DSC3(ii) **Wireless Networks**							
Course Type	Course Credit	Contact Hours/ Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: The Final Term examination shall cover the whole content of the course. The total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective-type questions from the complete syllabus. In addition to the compulsory first question, there shall be four units in the question paper each consisting of two questions. The student will attempt one question from each unit in addition to the compulsory question. All questions will carry equal marks.							
Course Objectives: To study fundamental concepts in wireless network, various LAN standards, IP and IPV6 Layer, Transmission protocols and WAN standards.							

Course Outcomes

At the end of this course, the student will be able to:

CO-1 Define: wireless LAN, architecture, mobile network layer, mobile transport layer and wireless wide area network.

CO-2 Describe: WLAN technologies, IEEE 802.11 types , IEEE 802.16, Bluetooth, IPV6, mobile ad-hoc network, TCP enhancements for wireless network, UTMS, 3G-MSC, 3G-SGSN, 3G-GGSN, applications of 4G, features and challenges of 5G.

CO-3 Illustrate: wireless LAN, system architecture, physical layer, Mac layer, Bluetooth architecture, mobile IP, mobile ad-hoc network, mobile transport layer, TCP improvements, wireless wide area network, HSDPA, features and challenges of 4G, 5G.

CO-4 Analyze: WLAN technologies, 802.11b, 802.11a, IEEE 802.16, IPV6, Routing, TCP enhancements, TCP improvements, UMTS core network architecture, firewall, 3G, 4G and 5G networks.

CO-5 Compare: different Wireless LAN technologies, mobile network layer, mobile transport layer, Mobile IP, mobile ad-hoc networks, protocols, TCP improvements and wireless WAN types.

CO-PO Mapping Matrix for Course MTech/ECE/2/DSC3(ii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	1	1	1	2	-	1	-	-	-	1	1
CO2	1	2	1	-	-	-	-	1	-	1	-	-
CO3	1	2	-	1	-	-	-	1	1	2	-	-
CO4	1	2	1	-	1	-	-	-	2	1	-	-
CO5	3	1	1	1	3	1	-	-	-	-	3	3

Unit – I

Wireless LAN: Introduction-WLAN technologies: Infrared, UHF narrowband, spread spectrum -IEEE802.11: System architecture, protocol architecture, physical layer, MAC layer, 802.11b, 802.11a – Hiper LAN: WATM, BRAN, HiperLAN2 – Bluetooth: Architecture, Radio Layer, Baseband layer, Link manager Protocol, security - IEEE802.16-WIMAX: Physical layer, MAC, Spectrum allocation for WIMAX.

Unit - II

Mobile Network Layer: Introduction - Mobile IP: IP packet delivery, Agent discovery, tunneling and encapsulation, IPV6- Network layer in the internet- Mobile IP session initiation protocol - mobile ad-hoc network: Routing, Destination Sequence distance vector, Dynamic source routing.

Unit - III

Mobile Transport Layer :TCP enhancements for wireless protocols - Traditional TCP: Congestion control, fast retransmit/fast recovery, Implications of mobility - Classical TCP improvements: Indirect TCP, Snooping TCP, Mobile TCP, Time out freezing, Selective retransmission, Transaction oriented TCP - TCP over 3G wireless networks.

Unit - IV

Wireless Wide Area Network: Overview of UTMS Terrestrial Radio access network-UMTS Core network Architecture: 3G-MSC, 3G-SGSN, 3G-GGSN, SMS-GMSC/SMS-IWMSC, Firewall, DNS/DHCP-High speed Downlink packet access (HSDPA)- LTE network architecture and protocol, features and challenges of 4G, Applications of 4G, Introduction to 5G vision,5G features and challenges.

Text/Reference Books

Text Books

1. Jochen Schiller “Mobile Communications”, 2e, Pearson Education 2012.
2. Vijay Garg “Wireless Communications and Networking”, 1e, Elsevier, 2007.

Reference Books

1. William Stallings, Wireless Communications and Networks, Pearson/Prentice Hall of India.
2. Erik Dahlman, Stefan Parkvall, Johan Skold and Per Beming, "3G Evolution HSPA and LTE for Mobile Broadband”, 2e, Academic Press, 2008.
3. Anurag Kumar, D. Manjunath, Joy Kuri, “Wireless Networking”, 1e, Elsevier 2011.
4. Simon Haykin, Michael Moher, David Koilpillai, “Modern Wireless Communications”, 1e, Pearson Education, 2013.

MTech/ECE/2/DSC3(iii) **Advancements in Communication Systems**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Course Objective

1. The objective of this course is to study about the advancement in communication systems.
2. Study about the digital communication & basic concepts of mobile communication.
3. Study of optical communication & multiplexing techniques.
4. To understand basics of navigation devices like Radar, Sonar.

Course Outcomes:

CO-1 Ability to understand about the advanced communication systems.
CO-2 Students get introduction about navigational techniques.
CO-3 Satellite is the core of modern communication. Students get the introduction about satellite by this subject.

CO-PO Mapping Matrix for Course MTech/ECE/2/DSC3(iii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	2	1	1	1	1	-	-	-	-	-	2
CO2	2	1	1	3	1	1	-	1	-	-	2	1
CO3	3	1	1	3	3	1	-	-	1	-	3	3

UNIT I

The essentials of a Communication system, Amplitude modulation, Phase modulation (PM) & frequency modulation (FM),Demodulation, ASK, FSK, BPSK, QPSK, Introduction to GSM, CDMA, Architecture of GSM, CDMA, Frequency Reuse concept, ISDN (Integrated Services digital Networks)

UNIT 2

Introduction to optical communication system: Electromagnetic spectrum used for optical communication, block diagram of optical communication system, Advantages of optical fiber communication, Optical fibers structures and their types, fiber characteristics, Basic principles of light propagation, Total internal reflection, Acceptance angle, Numerical aperture, Optical sources, Optical Detectors, Principles of optical detection, Optical Networks, why optical Networks? , SONET/SDH, WDM optical networks.

UNIT3

Communication signal multiplexing, Time division multiplexing, Frequency division multiplexing, Introduction to Multiple Access, FDMA, TDMA, Spread Spectrum multiple

Access, space division multiple access.

UNIT 4

Block Diagram and operation of RADAR, SONAR, Simple form of Radar Equation, Pulse Repetition frequency, VSAT(data broadband satellite), MSAT (Mobile Satellite Communication technique), Sarsat (Search & Rescue satellite) & LEOs (Lower earth orbit satellite), Satellite communication with respect to Fiber Optic Communication, LANDSAT, Defense satellite Beam Acquisition, Tracking & Positioning.

Text and Reference Books:

1. Communication systems (4th edn.): Simon Haykins; John wiley & sons.
2. Electronic Communication systems: Kennedy; TMH.
3. Optical Fiber Communications: John M Senior; PHI.
4. Wireless Communications: Theodore S. Rappaport; Pearsons.
5. Introduction to Radar Systems: Merrill I. Skolnik, ; MGH
6. Satellite Communication: D.C. Aggarwal; Khanna.

MTech/ECE/2/DSC4(i) **Embedded System for Wireless & Mobile Communication**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Communication system and Computer Networks

Course Objectives:

1. This elective course is a blend of the concepts developed in the core courses Embedded System design and Mobile Communication. This subject mainly focuses on the following objectives:
2. To develop basic understanding and impart in-depth knowledge of various topics like wireless communication technologies, Bluetooth protocol, its hardware, etc.
3. To introduce the concepts, architecture and programming related to JAVA.

Course Outcomes:

CO-1 Ability to develop basic understanding and impart in-depth knowledge of various topics like wireless communication technologies, Bluetooth protocol, its hardware, etc.

CO-2 Ability to understand the concepts, architecture and programming related to JAVA and various mobile applications.

CO-3 Ability to understand various kinds of antennas used for mobile applications.

CO-PO Mapping Matrix for Course MTech/ECE/2/DSC4(i)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	3	1	2	-	-	-	-	1	1
CO2	3	1	3	1	1	1	-	-	-	-	2	1
CO3	3	1	1	3	3	1	-	-	-	-	3	1

UNIT-1

Introduction to wireless technologies: WAP services, Serial and Parallel Communication, Asynchronous and synchronous Communication, FDM,TDM, TFM, Spread spectrum technology

UNIT-2

Introduction to Bluetooth: Specification, Core protocols, Cable replacement protocol. Bluetooth Radio: Type of Antenna, Antenna Parameters, Frequency hoping. Bluetooth Networking: Wireless networking, wireless network types, devices roles and states, adhoc network, scatternet.

UNIT-3

Connection establishment procedure, notable aspects of connection establishment, Mode of

connection, Bluetooth security, Security architecture, Security level of services, Profile and usage model: Generic access profile (GAP), SDA, Serial port profile, Secondary bluetooth profile
Hardware: Bluetooth Implementation, Baseband overview, packet format, Transmission buffers, Protocol Implementation: Link Manager Protocol, Logical Link Control Adaptation Protocol, Host control Interface, Protocol Interaction with layers

UNIT-4

Programming with Java: Java Programming, J2ME architecture, Javax. bluetooth package Interface, classes, exceptions, Javax.obex Package: interfaces, classes

Bluetooth services registration and search application, bluetooth client and server application. Overview of IrDA, HomeRF, Wireless LANs, JINI

Text Books:

1. Bluetooth Technology by C.S.R. Prabhu and A.P. Reddi; PHI

MTech/ECE/2/DSC4(ii) **Signal Processing**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Signal & System, Engineering Mathematics.

Course Objectives:

To introduce the concepts and techniques associated with the understanding of signal processing. To familiarize with techniques suitable for auditory perception and time delay estimation. To provide with an appreciation of applications for system modeling and identification.

Course Outcomes:

At the end of the semester, students will be able to:

CO-I Define & Describe the terminologies used in speech processing.

C0-2 Understand & explain various models for analysis of speech and audio signal

C0-3 Apply signal theory for the channel equalization, estimation

C0-4 Analyze & evaluate various equalization and TDE techniques in signal processing.

C0-5 Design various system and identify various models for Speech, TDE, Equalization & DOA

CO-PO Mapping Matrix for Course MTech/ECE/2/DSC4(ii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	1	1	1	1	-	-	-	-	1	3
CO2	2	1	1	3	1	1	-	-	-	-	2	3
CO3	3	1	1	3	3	1	-	-	-	-	3	3
CO4	3	3	1	3	1	1	-	-	-	-	3	3
CO5	3	1	1	1	3	1	-	-	-	-	3	3

UNIT-1

Speech and Audio Processing: Speech communication acoustic theory of speech: the source-filter model speech models and features. linear prediction models of speech harmonic plus noise model of speech fundamental frequency (pitch) information, speech coding, speech recognition, basic audio processing, hearing, psychoacoustics of hearing, speech analysis and classification, role of LPC coefficients in analysis filter. LPC stability issues.

UNIT-2

Time Delay Estimation: Need for the time delay estimation, system model, source localization strategies, ideal model-free field environment, TOE meth ods: cross-correlation function (CCF) method, least mean square (LMS) adaptive filter method, average square difference function (ASDF) method.

UNIT-3

Bayesian Inference and Channel Equalization:, Bayesian inference, basic definition, Bayesian theorem. elements of Bayesian inference, dynamics and probability model in estimation, parameter estimation and signal restoration, ML and MAP estimation, Introduction and need For Channel Equalization, Types of Equalization Techniques.

UNIT-4

System modeling and DOA: System identification based on FIR (MA), All Pole (AR), Pole Zero (ARMA) system models, Basic Principle of DOA Estimation, Need of DOA, Beam forming, Direction of Arrival OAf, Estimation Algorithms.

Text Books:

1. Simon S Haykins "Adaptive Filter Theory" PHI, 3rd Edition
2. Proakis "Digital Signal Processing" PHT 2nd edition

MTech/ECE/2/DSC4(iii) **MEMS and IC Integration**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: IC Fabrication Technology, Analog and Digital VLSI Design

Course Objectives:

This course has been developed due to industry request and as an introduction to a growing and important field in our high technology future. The objectives of this course are to teach critical thinking in micro engineering process, materials and design issues, to build an understanding of micro scale physics for use in designing MEMS applications, review current MEMS, RFMEMS and Bio MEMS applications, use the above knowledge to design and fabricate novel EMS/Bio MEMS /RF MEMS applications as part of a group project.

Course Outcomes:

CO-1 Ability to Understand CMOS IC fabrication and MEMS applications.

CO-2 Ability to understand the use of a new set of design and verification tools, in addition to AutoCAD tools.

CO-3 Ability to understand the materials and processes used to design and fabricate MEMS

CO-PO Mapping Matrix for Course MTech/ECE/2/DSC4(iii)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	2	1	1	1	1	-	-	-	-	1	3
CO2	2	2	1	3	2	1	-	-	-	-	2	3
CO3	3	1	2	3	3	2	-	-	-	-	3	3

UNIT-1

MEMS Fabrication:

Conventional MEMS fabrication using VLSI technology: lithography, chemical etching: isotropic and anisotropic, Plasma etching, Reactive ion etching, Oxidation, Chemical vapor deposition, LPCVD, PECVD, Surface micromachining, LIGA, single layer and higher layer fabrication, Non-conventional MEMS fabrication: laser micromachining and welding micromachining(EDM & ECM), Microstereolithography: scanning process, dynamic mask process, Electronic packaging.

UNIT-2

MEMS Design and Analysis:

Basic concepts of design of MEMS devices and processes, Design for fabrication, Other design

considerations, Analysis of MEMS devices, Modeling and Simulation.

UNIT-3

MEMS Sensors:

Physical Micro Sensors: Classification of physical sensors, Integrated, Intelligent, or Smart Sensors, Sensor Principles and Examples: Thermal Sensors, Electrical Sensor, Mechanical Sensors, Chemical and Biosensors, Application Areas: RF MEMS and Optical MEMS, Medical Devices e.g. DNA-chip, micro-arrays, Pressure sensors with embedded electronics(Analog/Mixed signal): Accelerometer with transducer, Gyroscope, Bolo meter design.

UNIT-4

MEMS Characterization:

Technologies for MEMS characterization, Scanning Probe Microscopy (SPM), Atomic Force Microscopy (AFM), Scanning Tunneling Microscopy (STM), Magnetic Force Microscopy, Scanning Electron Microscope.

Text/Reference Books:

1. Gregory T.A. Kovacs, Micromachined Transducers Sourecbook, The McGraw-Hill, Inc. 1998
2. Stephen D. Senturia, Microsystem Design, Kluar Publishers, 2001
3. NadimMaluf, An Introduction to Microelectromechanical Systems Engineering, Artech House, 2000.
4. M.H. Bao, Micro Mechanical Transducers, Volume 8, Handbook of Sensors and Actuators, Elsevier, 2000.
5. MasoodTabib-Azar, Microactuators, Kluwer, 1998.
6. LjubisaRistic, Editor, Sensor Technology and Devices, Artech House, 1994
7. D. S. Ballantine, et. al., Acoustic Wave Sensors, Academic Press, 1997
8. H. J. De Los Santos, Introduction to Microelectromechanical (MEM) Microwave Systems, Artech, 1999.
9. James M.Gere and Stephen P. Timoshenko, Mechanics of Materials, 2nd Edition, Brooks/Cole Engineering Division, 1984

Third Semester

MTech/ECE/3/CC9 **Advanced Digital Communication**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Compulsory Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Communication system

Course Objectives:

The aim of this subject is to develop a thorough understanding of the main concepts, techniques and performance criteria used in the analysis and design of digital communication systems.

Topics include:-

1. Introduction of digital communication system.
2. Digital modulation techniques.
3. Reception of digital signal.
4. Information theory and coding.

Course Outcomes:

After completion of the course, the student will be able to

CO-1 Ability to understand the working principles of existing and advanced digital communication techniques.

CO-2 Ability to understand basic techniques suitable to understand, design and evaluate the main elements of a modern digital communication system.

CO-3 Ability to recognize the broad applicability of digital communication systems in society

CO-PO Mapping Matrix for Course MTech/ECE/3/CC9

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	1	2	1	-	-	1	-	-	3	3
CO2	3	1	1	2	3	-	-	2	-	-	3	3
CO3	3	3	3	3	3	-	-	-	-	1	3	3

UNIT-1

Introduction: Elements of Digital Communication system, Bandpass and Lowpass signal representation, Comparison between analog & Digital Communication, Performance parameters of Digital Communication, Concept of Constellation, BER, etc.

UNIT-2

Digital Modulation Techniques: Mathematical expressions, transmitter & receiver structure of ASK, FSK, BPSK, QPSK, M-ary PSK, MSK, QAM.

UNIT-3

Reception of Digital Signal: Baseband signal reception, Probability of error, Optimum filter

receiver, Matched filter receiver, Coherent reception, calculation of error probability for PSK, MSK, ISI, Pulse Shaping Techniques.

UNIT-4

Information Theory & Coding: Measures of information, Entropy, Information rate, Channel Capacity, Source Coding (Huffman, Shannon-Fano, Lempel-Ziv), Channel coding (Block codes, Convolution codes, Turbo codes).

Text Books:

1. Digital Communications by J.G Proakis & M Salehi, 5th Edition McGraw Hill
2. Principle of Communication systems –Taub&Schilling,TataMcGraw Hill
3. Digital Communication –Simon Haykins,John Wiley & Sons.
4. Digital Communications: Fundamentals and applications- Bernard Sklar, PHI
5. B.P.Lathi,Modern Digital and analog communication systems,3rd Edition, Oxford
6. University Press,1998.

MTech/ECE/3/CC10 **Research Methodology**							
Course Type	Course Credit	Contact Hours/ Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Compulsory Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: The Final Term examination shall cover the whole content of the course. The total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective-type questions from the complete syllabus. In addition to the compulsory first question, there shall be four units in the question paper each consisting of two questions. The student will attempt one question from each unit in addition to the compulsory question. All questions will carry equal marks.							
Course Objectives: The objective of this course is to get the students familiar with different aspects of research methodology, namely, research design, collection and analysis of data, and interpretation of results.							

Course Outcomes

At the end of this course, the student will be able to :

CO-1 define: objectives, hypothesis, interpretation, data analysis, data collection, research design and method, interpretation, data analysis, sampling.

CO-2 describe: objectives, hypothesis, interpretation, data analysis, data collection, research design and method, interpretation, data analysis, sampling.

CO-3 Illustrate: measurement. data collection, processing, sampling, analysis and its strategies, reports.

CO-4 categorize: research, sampling methods, data collection techniques, reports ,and data processing strategies,
perform: data analysis.

CO-5 compare: sampling methods, data collection techniques, reports and data processing strategies.

CO-6 create: thesis, reports, design: research tool , interpret(drive): results

CO-PO Mapping Matrix for Course MTech/ECE/3/CC10												
Cos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	2	1	1	-	-	-	-	1	1	1
CO2	2	1	1	3	1	-	-	-	-	2	2	2
CO3	3	1	3	3	2	-	-	1	-	2	3	2
CO4	2	3	1	2	1	-	-	1	-	-	3	3
CO5	3	1	1	2	3	-	-	2	-	-	3	3
CO6	3	3	3	3	3	-	-	-	-	1	3	3

Unit – I

Objectives and types of research: motivation and objectives- research methods vs. methodology, types of research- descriptive vs. analytical, applied vs. fundamental, quantitative vs. qualitative, conceptual vs empirical research formulation: defining and formulating the research problem-. selecting the problem, necessity of defining the problem, importance of literature review in defining a problem, literature review-primary and secondary source reviews, hypothesis- definition, qualities of a good hypothesis, null hypothesis and alternatives.

Unit – II

Research design and methods: basic principles, need of research design- features of good design, important concepts relating to research design, criteria of selecting a sampling procedure, characteristics of a good sample design, sampling methods, measurement: concept of measurement, problems in measurement in research - validity and reliability. levels of measurement- nominal, ordinal, interval, ratio.

Unit – III

Data collection and analysis: execution of the research, observation and collection of data, methods of data collection, data processing and analysis strategies, data analysis with statistical packages, hypothesis testing, generalization and interpretation, univariate analysis (frequency tables, bar charts, pie charts, percentages).

Unit – IV

Meaning of interpretation, need of interpretation, technique of interpretation, precaution in interpretation, layout of a research paper, journals in computer science, impact factor of journals, ethical issues related to publishing, plagiarism and self-plagiarism. reports and thesis writing: structure and components of scientific reports, types of report- technical reports and thesis, writing-synopsis, abstract, illustrations and tables, results, summary, reference citing and listing

Text/Reference Books

Text Books

1. J. Garg, B.L, Karadia, R, Aggarwal F, An Introduction to Research Methodology, RBSA Publishers, 2002.
2. Kothari, C.R, Research Methodology: Methods and Techniques. New Age International, 1990
3. Santosh Gupta, Research Methodology and Statistical Techniques, Deep & Deep Publications Pvt. Ltd., 2008

Reference Books

1. N. Gurumani, Scientific Thesis Writing and Paper Presentation, MJP Publishers. Montgomery, Douglas C, Design and Analysis of Experiments, Wiley India Pvt. Ltd

MTech/ECE/3/CC11 **Communication System Design Lab**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Practical	02	04	Lab Work	50	-	3 Hours	TEE/ Practical File
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Communication System

Course Objectives: The course provides an overview of optical communication, particularly fibre optics and deals with both the function of related components and with system performance. Various basic structures like wired, wireless, wireless sensor and adhoc network etc. also analysed at the end of the course.

Course Outcomes:

CO-1 To demonstrate and design WDM high bit-rate fibre optic communication systems.

CO-2 To analyse, model and implement advanced optical communication systems.

CO-3 To use optical communications simulation tools to assess the results obtained from theoretical studies.

CO-PO Mapping Matrix for Course MTech/ECE/3/CC11

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	3	2	1	1	2	-	-	-	-	1	3
CO2	2	1	3	3	1	1	-	-	-	-	2	3
CO3	3	1	2	3	3	1	-	-	-	-	3	3

List of Experiments

1. To study dispersion with and without compensation.
2. To study BER (Bit error rate) in optical transmitter link of 100 Km.
3. To study four channels WDM using computer system using two spans of dispersion shifted fiber of opposite dispersion value.
4. To study DQPSK modulation technique using RZ pattern.
5. To study fiber linear effects (Polarization mode dispersion).
6. To study fiber non-linear effects (self-phase modulation).
7. To study fiber non-linear effects using cross phase modulation (XPM).

Note: This list is an indicative list of experiments, which can be expanded depending on the course requirement.

MTech/ECE 3/SEC1:Dissertation Part-1							
Course Type	Course Credit	Contact Hours/ Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Research Work	4	04	-	-	100	-	Teacher interaction/ Presentation
Instructions to paper setter for Final Term Examination: The Final Term examination will be conducted by internal examiner. Examinees will be evaluated on the bases of interaction and presentation.							

Pre-requisites: Knowledge of research area

Course Objective: The objective is to enhance the research abilities of PG students. The aim is always kept into mind that any research that is done must be implemented to the day to day life. It must add up some ease in the life of a common man and benefit of the society. The students are asked to make a detailed literature survey of field of choice and formulate the problem to work on.

Course Outcomes:

CO-1 Ability to identify research issue/problem on complex engineering topics related to ECE.
CO-2 Gain knowledge on the research problem identified through extensive literature survey.
CO-3 Ability to work in group and mange and understand research papers/literature related to research topic through group-discussion.
CO-4 Understanding of professional & ethical research issues.
CO-5 Ability to present/communicate effectively the research topic though synopsis presentation.
CO-6 Understanding of simulator tools required to carry out research work.

CO-PO Mapping Matrix for Course MTech/ECE 3/SEC1

Cos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	2	-	-	-	-	3	2	3	3
CO2	2	1	-	1	1	-	-	-	1	2	2	3
CO3	1	2	1	1	-	-	-	-	1	1	2	2
CO4	3	2	2	3	-	-	-	1	1	3	2	2
CO5	1	3	1	1	1	1	1	-	-	-	1	3
CO6	2	1	1	3	1	1	-	-	-	-	2	3

The Thesis work should be of Research nature only and it should be started during the third semester and the candidate must do the following:

a) Literature Survey
b) Problem Formulation

Around 40% of the Thesis work should be completed in this semester. The remaining 60% work will be carried out in the fourth semester. Each student is required to submit a detailed report about the work done on topic of Thesis as per the guidelines decided by the department. The Thesis work is to be evaluated through Presentations and Viva-Voce during the semester and at the end of semester as per the guidelines decided by the department from time to time.

Fourth Semester

MTech/ECE4/SEC2:Dissertation Part-2							
Course Type	Course Credit	Contact Hours/ Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Research Work	16	04	-	300	-	-	Presentation, Dissertation &Viva-Voce
Instructions to paper setter for Final Term Examination: The Final Term examination will be conducted by external examiner. Examinees will be evaluated on the bases of presentation, Dissertation and Viva-Voce.							

Pre-requisites: Knowledge of Basic domain

Course Objective: Research is the back of scientific and social growth of any country and specially the research that is related to the day to day life. The PG students are motivated to use their accumulated knowledge for such research that adds up some ease in the life of a common man and beneficial for the society. The students get the knowledge of state of art technology in their field and start working.

Course Outcomes:

CO-1 Ability to bring ideas into practice through simulation of analysis of research topic.
CO-2 Ability to identify specific problems/issues in the form of research objectives.
CO-3 Ability to propose a novel idea/modified technique/new interpretation after analyzing the existing research work.
CO-4 Ability to contribute towards the knowledge up gradation of scientific community and society in general.
CO-5 Imposed communication skills (oral as well as writing) through seminars, group discussions, thesis writing and research paper writing.
CO-6 Understating of significance of ethical and research professional.
CO-7 Ability to stay updated through continuous learning.
CO-8 Understanding of research techniques and simulation tools for detected analysis of research issues.
CO-9 Interpretation and compilation of simulation result to issue at a meaningful conclusion.

CO-PO Mapping Matrix for Course MTech/ECE4/SEC2												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	1	1	1	2	-	-	-	-	3	2	3	3
CO2	2	1	-	1	1	-	-	-	1	2	2	3
CO3	1	2	1	1	-	-	-	-	1	1	2	2
CO4	3	2	2	3	-	-	-	1	1	3	2	2
CO5	1	3	1	1	1	1	1	-	-	-	1	3
CO6	2	1	1	3	1	1	-	-	-	-	2	3
CO7	3	1	1	3	3	1	-	-	-	-	3	3
CO8	3	3	1	3	1	1	-	-	-	-	3	3
CO9	3	1	1	1	3	1	-	-	-	-	3	3

Around 40% of the Thesis work should be completed in third semester. The remaining 60% work will be carried out in this semester. Each student is required to submit a detailed Thesis report about the work done (III Sem + IV Sem) on topic of Thesis as per the guidelines decided by the department. The Thesis work is to be evaluated through Presentations and Viva-Voce during the semester and Final evaluation will be done at the end of semester as per the guidelines decided by the department from time to time.

The candidate has to present/publish one paper in national/international conference/seminar/journal of repute before final submission. Research work should be carried out at parent institute. However candidate may visit research labs/institutions with the due permission of Head of the Department on recommendation of supervisor concerned.

Open Elective subjects offered to other departments

ECE/OEC1 **Advancements in Communication Systems**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Course Objectives:

1. The objective of this course is to study about the advancement in communication systems.
2. Study about the digital communication & basic concepts of mobile communication.
3. Study of optical communication & multiplexing techniques.
4. To understand basics of navigation devices like Radar, Sonar.

Course Outcomes:

CO-1 Ability to understand about the advanced communication systems.
CO-2 Students get introduction about navigational techniques.
CO-3 Satellite is the core of modern communication. Students get the introduction about satellite by this subject.

CO-PO Mapping Matrix for Course ECE/OEC(i)												
COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	2	3	3	3	2	-	1	-	-	-	1	1
CO2	1	2	1	-	-	-	2	1	2	1	-	-
CO3	2	3	-	1	-	-	-	1	1	2	-	-

UNIT I

The essentials of a Communication system, Amplitude modulation, Phase modulation (PM) & frequency modulation (FM),Demodulation, ASK, FSK, BPSK, QPSK, Introduction to GSM, CDMA, Architecture of GSM, CDMA, Frequency Reuse concept, ISDN (Integrated Services digital Networks)

UNIT 2

Introduction to optical communication system: Electromagnetic spectrum used for optical communication, block diagram of optical communication system, Advantages of optical fiber communication, Optical fibers structures and their types, fiber characteristics, Basic principles of light propagation, Total internal reflection, Acceptance angle, Numerical aperture, Optical sources, Optical Detectors, Principles of optical detection, Optical Networks, why optical Networks? , SONET/SDH, WDM optical networks.

UNIT3

Communication signal multiplexing, Time division multiplexing, Frequency division multiplexing, Introduction to Multiple Access, FDMA, TDMA, Spread Spectrum multiple Access, space division multiple access.

UNIT 4

Block Diagram and operation of RADAR, SONAR, Simple form of Radar Equation, Pulse Repetition frequency, VSAT(data broadband satellite), MSAT (Mobile Satellite Communication technique), Sarsat (Search & Rescue satellite) & LEOs (Lower earth orbit satellite), Satellite communication with respect to Fiber Optic Communication, LANDSAT, Defense satellite Beam Acquisition, Tracking & Positioning.

Text and Reference Books:

1. Communication systems (4th edn.): Simon Haykins; John wiley & sons.
2. Electronic Communication systems: Kennedy; TMH.
3. Optical Fiber Communications: John M Senior; PHI.
4. Wireless Communications: Theodore S. Rappaport; Pearsons.
5. Introduction to Radar Systems: Merrill I. Skolnik, ; MGH

ECE/OEC2 **WIRELESS COMMUNICATION**							
Course Type	Course Credit	Contact Hours/Week	Delivery Mode	Maximum Marks		Exam Duration	Assessment Methods
				External	Internal		
Optional Theory	04	04	Lecture	70	30	3 Hours	TEE/MTE/ Assignment/ Attendance
Instructions to paper setter for Final Term Examination: Final Term examination shall cover the whole content of the course. Total number of questions shall be nine. Question number one will be compulsory and will be consisting of short/objective type questions from complete syllabus. In addition to compulsory first question there shall be four units in the question paper each consisting of two questions. Student will attempt one question from each unit in addition to compulsory question. All questions will carry equal marks.							

Pre-requisites: Communication System

Course Objectives:

1. To develop basic understanding and impart in-depth knowledge of various concepts used in wireless mobile communication.
2. To introduce the concepts, parameters and models of mobile radio propagation.
3. To help students understand the architecture and elements of wireless standards and systems like GSM, GPRS, CDMA, etc.
4. To provide coverage to the advanced, latest and upcoming wireless technologies like OFDM, Multicarrier Modulation and 4G.

Course Outcomes:

At the end of the semester, students will be able:

CO-1 To describe the evolution & advancements in wireless networks.
CO-2 To explain the operation of cellular networks.
CO-3 To define the channel behaviour and associated losses.
CO-4 To evaluate the performance of cellular networks.

CO-PO Mapping Matrix for Course ECE/OEC2

COs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
CO1	3	3	1	1	1	1	-	-	1	-	-	1
CO2	2	1	-	1	1	1	-	-	-	-		
CO3	2	1	1	1	3	1	-	-	-	-		
CO4	3	3	3	2	1	1	-	-	-	-		

UNIT-1

INTRODUCTION: Introduction to Generation of Wireless communication systems- 1G, 2G, 3G, 4G, 5G. Examples of various wireless communication systems: paging system, Wireless Local Loop, Bluetooth, Introduction to frequency bands for radio transmission, Applications of wireless communication.

UNIT-II

CELLULAR SYSTEM: The Cellular concept, Frequency Reuse, basic theory of hexagonal cell layout, Frequency Management and Channel Assignment, Call drops, hand off, types of handoff, Method to improve capacity, Call Control, Mobility Management and location Tracing, Erlang capacity comparison.

UNIT –III

PATH LOSS ANALYSIS: Models for Path loss: Free space propagation, Okumura model, Hata model, Longley-Rice model, PCS extension to Hata model, Partition loss modelling, Log distance path loss model, Ericsson multiple breakpoint model. Concept of coherence bandwidth, coherence time & Doppler spread. Types of fading: Flat fading, frequency selective fading, fast fading, slow fading. Diversity techniques in mobile radio.

UNIT-IV

MULTIPLE ACCESS TECHNIQUES & WIRELESS STANDARDS: Multiple Access Techniques used in Mobile Wireless Communications: FDMA, TDMA, CDMA, SSMA, cellular CDMA & its capacity, Rake receiver.

GSM & GPRS STANDARD: Architecture, channels, RF specifications. IS-95 standard: architecture, channels, RF specifications. Introduction to WCDMA, OFDM, LTE, 5G Technology: Basic architecture/ block diagram, RF specifications, applications.

TEXT BOOKS:

1. Theodore S. Rappaport, Wireless Communications Principles and Practice, IEEE Press, Prentice Hall.
2. William C.Y.Lec, Mobile Cellular Telecommunications, Analog and Digital Systems, McGraw Hill Inc.

REFERENCE BOOKS:

1. Mobile Communication Hand Book, 2nd Ed., IEEE Press.
2. Wireless Communications, TL Singal, McGraw Hill (India).
3. Wireless and personal Communication Systems by VK Garg and JE Wilkes; Prentice Hall, 1996.
4. Mobile and Personal Communication Systems and Services, Raj Pandya, Wiley IEEE Press.